Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-20 are pending in the application, with claims 1, 7, 13, 15, 17, and 18-20 being the independent claims. Claims 1, 7, 13, 15, 17, and 18-20 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejections Under 35 U.S.C. § 102

Dhong

The Office Action rejected claims 13 and 14 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,816,706 to Dhong *et al.* (hereinafter "Dhong"). (*See*, Office Action at p. 2.) Applicants respectfully traverse these rejections.

Amended independent claim 13 recites (emphasis added):

> A reset circuit for a latch circuit having a bistable pair of transistors, the reset circuit comprising:
>
> a first transistor connected to a supply voltage at a first node;
>
> a second transistor connected to said first transistor ***at a second node*** and to a first port of the latch circuit, wherein a gate terminal of said second transistor is connected to a drain terminal of said second transistor at said first port; and
>
> a third transistor connected to said first transistor ***at said second node*** and to a second port of the latch circuit, wherein a gate terminal of said third transistor is connected to a drain terminal of said third transistor at said second port;

> wherein transistors of said latch circuit, said first transistor, said second transistor, and said third transistor are all characterized by a common channel type, said common channel type being one of a p-channel type and a n-channel type.

Dhong does not disclose, teach, or suggest a reset circuit having a first transistor, a second transistor, a third transistor in which the first transistor is connected to a supply voltage at a first node, the second transistor is connected to the first transistor at a second node, and the third transistor is connected to the first transistor at the second node. Therefore, Dhong does not anticipate claim 13. Likewise, claim 14, which depends upon claim 13, is not anticipated by Dhong. Claim 14 is also allowable because of its additional distinctive features. Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 13 and 14 under 35 U.S.C. § 102(e) with respect to Dhong.

Opris

The Office Action rejected claims 7 and 9-12 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,060,912 to Opris *et al.* (hereinafter "Opris"). (*See*, Office Action at p. 3.) Applicants respectfully traverse these rejections.

Amended independent claim 7 recites (emphasis added):

> A latch circuit, comprising:
>
> a bistable pair of transistors connected between a reset switch and a first supply voltage, and having a first port for receiving a first current signal and producing a first output voltage, and a second port for receiving a second current signal and producing a second output voltage; and
>
> a vertical latch connected between said first supply voltage and a second supply voltage, and connected to said first port;
>
> wherein said vertical latch comprises:
>
> a first current mirror pair connected ***at a node to said first port;*** and

a second current mirror pair connected ***at said node to said first port.***

Opris does not disclose, teach, or suggest a latch circuit comprising a bistable pair of transistors and a vertical latch in which the vertical latch has a first current mirror pair connected to a first port of the latch circuit at a node and a second current mirror pair connected to the first port of the latch circuit at the node. Therefore, Opris does not anticipate claim 7. Likewise, claims 9-12, which depend upon claim 7, is not anticipated by Opris. Claims 9-12 are also allowable because of their additional distinctive features. Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 7 and 9-12 under 35 U.S.C. § 102(b) with respect to Opris.

Ang

The Office Action rejected claims 1-6 and 15-20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,147,515 to Ang *et al.* (hereinafter "Ang"). (*See*, Office Action at p. 4.) Applicants respectfully traverse these rejections.

Regarding claims 1-6, amended independent claim 1 recites (emphasis added):

> A latch circuit, comprising:
>
> a bistable pair of transistors connected between a reset switch and a first supply voltage, and having a first port for receiving a first current signal and producing a first output voltage, and a second port for receiving a second current signal and producing a second output voltage; and
>
> a vertical latch connected between said first supply voltage and a second supply voltage, and connected to said first port, said vertical latch having ***a transistor connected to said first port so that, when said transistor is turned on, a current flows from said second supply voltage through said transistor to said first port.***

Ang does not disclose, teach, or suggest a latch circuit having a bistable pair of transistors connected between a reset switch and a first supply voltage, and a vertical

latch connected between the first supply voltage and a second supply voltage and connected to a first port of the bistable pair of transistors so that, when the transistor is turned on, a current flows from the second supply voltage through the transistor to the first port. Therefore, Ang does not anticipate claim 1. Likewise, claims 2-6, which depend upon claim 1, are not anticipated by Ang. Claims 2-6 are also allowable because of their additional distinctive features. Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 1-6 under 35 U.S.C. § 102(e) with respect to Ang.

Regarding claims 15 and 16, amended independent claim 15 recites (emphasis added):

> An analog-to-digital converter, comprising:
>
> a comparator having a first input for receiving an analog signal and a second input for receiving a reference signal, said comparator for producing a digital signal;
>
> wherein said comparator comprises a latch circuit having a bistable pair of transistors coupled between a reset circuit and a first supply voltage, and a vertical latch coupled between said first supply voltage and a second supply voltage and coupled to said bistable pair of transistors at a node coupled to said reset circuit, said vertical latch having a first transistor and a second transistor, said first transistor being of a first channel type, said second transistor being of a second channel type, said first channel type being one of a p-channel type and a n-channel type, said second channel type being different from said first channel type, and ***said first transistor is coupled to said bistable pair of transistors at said node so that, when said first transistor is turned on, a current flows from said second supply voltage through said first transistor to said node.***

Ang does not disclose, teach, or suggest a latch circuit having a bistable pair of transistors coupled between a reset circuit and a first supply voltage, and a vertical latch coupled between the first supply voltage and a second supply voltage and coupled to the bistable pair of transistors at a node coupled to the reset circuit, wherein the latch circuit

has a first transistor and a second transistor and the first transistor is coupled to the bistable pair of transistors at the node so that, when the first transistor is turned on, a current flows from the second supply voltage through the first transistor to the node. Therefore, Ang does not anticipate claim 15. Likewise, claim 16, which depends upon claim 15, is not anticipated by Ang. Claim 16 is also allowable because of its additional distinctive features. Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 15 and 16 under 35 U.S.C. § 102(e) with respect to Ang.

Regarding claim 17, amended independent claim 17 recites (emphasis added):

> In a latch circuit, a method for decreasing the time in which a first latch circuit port receiving a current signal greater than a bias current reaches a first steady state voltage, comprising the steps of:
>
> (1) amplifying the current signal greater than the bias current; and
>
> (2) applying said amplified current signal to the first latch circuit port;
>
> ***wherein the first steady state voltage is a high voltage, a second steady state voltage of a second latch circuit port receiving a current signal less than the bias current is a low voltage, and the first latch circuit port and the second latch circuit port are at a middle voltage when a reset circuit couples the first latch circuit port to the second latch circuit port.***

Ang does not disclose, teach, or suggest a latch circuit in which a first latch circuit port and a second latch circuit port are at a middle voltage when a reset circuit couples the first latch circuit port to the second latch circuit port. To the contrary, Ang, at column 5, lines 54-64 recites:

> In operation, when the clock signal L1CLK is low, resolving circuit **200** is off (i.e., unpowered) and equalization circuit **209** is on. Accordingly, the nodes SENS and SENSB are both coupled to ground. Because the nodes SENS and SENSB are coupled to ground, output-stage transistors **231**, **233**, **235** and **237** of latch circuit **202** are off. However, transistors **244** and **246** are coupled to VDD and thus latch circuit **202** is on despite the

> clock signal being low. Accordingly, latching circuit **202** holds its previous value and the OUT signal is maintained as the previous value held in latching circuit **202**.

Therefore, Ang does not anticipate claim 17. Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejection of claim 17 under 35 U.S.C. § 102(e) with respect to Ang.

Regarding claims 18-20, amended independent claim 18 recites (emphasis added):

> In a latch circuit having a bistable pair and a vertical latch, a method for reducing the power consumed by the latch circuit, comprising the steps of:
>
> (1) resetting the bistable pair and the vertical latch; and
>
> (2) holding a fourth transistor OFF during said resetting;
>
> wherein the bistable pair has a first transistor and a second transistor configured so that a first type terminal of the first transistor is connected to a second type terminal of the second transistor at a first port, the first type terminal of the second transistor is connected to the second type terminal of the first transistor at a second port, and a third type terminal of the first transistor and the third type terminal of the second transistor are connected together, and wherein the vertical latch has a third transistor and the fourth transistor configured so that the second type terminal of the third transistor is connected ***at a first node*** to the second type terminal of the second transistor and to the first type terminal of the fourth transistor, the third type terminal of the third transistor is connected to a first supply voltage, the third type terminal of the fourth transistor is connected at a second node to a second supply voltage, and the second type terminal of the fourth transistor is connected to the first type terminal of the third transistor.

Each of claims 19 and 20 have been amended to have an independent form and to recite features similar to those of independent claim 18.

Ang does not disclose, teach, or suggest a bistable pair having a first transistor and a second transistor and a vertical latch having a third transistor and a fourth transistor, wherein a first type terminal of the first transistor is connected to a second type terminal of the second transistor at a first port, the first type terminal of the second

transistor is connected to the second type terminal of the first transistor at a second port, and the second type terminal of the third transistor is connected at a first node to the second type terminal of the second transistor and to the first type terminal of the fourth transistor. Therefore, Ang does not anticipate any of claims 18, 19, or 20. Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 18-20 under 35 U.S.C. § 102(e) with respect to Ang.

Shiratake

The Office Action rejected claims 18-20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,147,514 to Shiratake (hereinafter "Shiratake"). (*See*, Office Action at p. 6.) Applicants respectfully traverse these rejections.

Regarding claims 18-20, amended independent claim 18 recites (emphasis added):

> In a latch circuit having a bistable pair and a vertical latch, a method for reducing the power consumed by the latch circuit, comprising the steps of:
>
> (1) resetting the bistable pair and the vertical latch; and
>
> (2) holding a fourth transistor OFF during said resetting;
>
> wherein the bistable pair has a first transistor and a second transistor configured so that a first type terminal of the first transistor is connected to a second type terminal of the second transistor at a first port, the first type terminal of the second transistor is connected to the second type terminal of the first transistor at a second port, and a third type terminal of the first transistor and the third type terminal of the second transistor are connected together, and wherein the vertical latch has a third transistor and the fourth transistor configured so that the second type terminal of the third transistor is connected at a first node to the second type terminal of the second transistor and to the first type terminal of the fourth transistor, the third type terminal of the third transistor is connected to a first supply voltage, the third type terminal of the fourth transistor is connected to a second supply voltage, and the second type terminal of the fourth transistor is connected ***at a second node*** to the first type terminal of the third transistor.

Each of claims 19 and 20 have been amended to have an independent form and to recite features similar to those of independent claim 18.

Shiratake does not disclose, teach, or suggest a bistable pair having a first transistor and a second transistor and a vertical latch having a third transistor and a fourth transistor, wherein a first type terminal of the first transistor is connected to a second type terminal of the second transistor at a first port, the first type terminal of the second transistor is connected to the second type terminal of the first transistor at a second port, and the second type terminal of the fourth transistor is connected at a second node to the first type terminal of the third transistor. Therefore, Ang does not anticipate any of claims 18, 19, or 20. Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 18-20 under 35 U.S.C. § 102(e) with respect to Ang.

Rejections Under 35 U.S.C. § 103

The Office Action rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Opris. (*See*, Office Action at p. 7.) Applicants respectfully traverse this rejection. Claim 8 is dependent upon claim 7. As stated above, Opris does not disclose, teach, or suggest a latch circuit comprising a bistable pair of transistors and a vertical latch in which the vertical latch has a first current mirror pair connected to a first port of the latch circuit at a node and a second current mirror pair connected to the first port of the latch circuit at the node. Therefore, claims 7 and 8 are patentable over Opris.

Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejection of claim 8 under 35 U.S.C. § 103(a) with respect to Opris.

Conclusion

All of the stated grounds of rejection have been properly traversed. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Timothy A. Doyle

Timothy A. Doyle
Attorney for Applicants
Registration No. 51,262

Date: 7 NOV 05

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

436430_1.DOC